



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,763	02/13/2006	Amina Hamidi	004501-820	4261
21839	7590	03/12/2009		
BUCHANAN, INGERSOLL & ROONEY PC POST OFFICE BOX 1404 ALEXANDRIA, VA 22313-1404			EXAMINER NGUYEN, KHIEM D	
			ART UNIT 2823	PAPER NUMBER
			NOTIFICATION DATE 03/12/2009	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

### Office Action Summary

**Application No.**

10/551,763

**Applicant(s)**

HAMIDI ET AL.

**Examiner**

KHIEM D. NGUYEN

**Art Unit**

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14 and 15 is/are allowed.
- 6) ☒ Claim(s) 7, 8, 13 and 16-19 is/are rejected.
- 7) ☒ Claim(s) 9-12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB-08)  
Paper No(s)/Mail Date 07/30/08
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Remarks*

1. The Amendment filed on January 01<sup>st</sup>,2009 is acknowledged. Claims 9 and 11 have been amended and Claims 16-19 are newly added. Accordingly, Claims 7-19 are pending in the present application.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

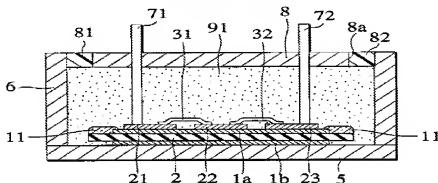
3. Claims 7, 8, 13, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072), both of record.

In re claim 7, Shimizu et al. disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

at least one semiconductor power chip **21/23** mounted on said first electrically conductive layer **1a** (see col. 12, lines 6-8);

a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B));

FIG.2A

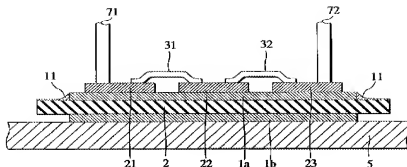


a second insulating material **91** at least partially embedding said semiconductor power chip **21/23**, said electrically insulating substrate **2**, said first electrically conductive layer **1a**, and said first electrically insulating material **11** (col. 11, lines 58-62 and FIG. 2A, for example);

wherein the first electrically insulating material **11** is an epoxy resin or polyester resin (col. 12, lines 49-58), and

the surface of the first electrically insulating material **11** disposed in the corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example).

FIG.2B



However, Shimizu et al. is silent about wherein the first electrically insulating material is a polyimide.

Nidan et al. discloses wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As Nidan et al. disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin as taught by Nidan et al. since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

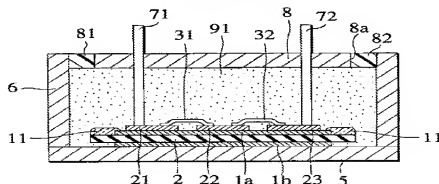
In re claim 8, as applied to claim 7 above, Shimizu et al. in combination with Nidan et al. discloses all claimed limitations including the limitation wherein the electrically insulating substrate **2** is mounted on a bottom plate **5** (see col. 12, lines 9-13 and FIG. 2A, for example).

In re claim 13, Shimizu et al. disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

at least one semiconductor power chip **21/23** mounted on said first electrically conductive layer **1a** (see col. 12, lines 6-8);

a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B));

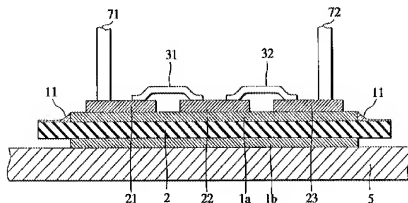
FIG.2A



a second insulating material **91** at least partially embedding said semiconductor power chip **21/23**, said electrically insulating substrate **2**, said first electrically conductive layer **1a**, and said first electrically insulating material **11** (col. 11, lines 58-62 and FIG. 2A, for example); wherein the first electrically insulating material **11** is a epoxy resin or polyester resin (col. 12, lines 49-58), and

the surface of the first electrically insulating material **11** disposed in the corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example),

**FIG.2B**



wherein the first electrically insulating material **11** fills gaps in a junction between the first electrically conductive layer **1a** and the electrically insulating substrate **2** (see col. 12, lines 49-63 and FIG. 2A).

However, Shimizu et al. is silent about wherein the first electrically insulating material is a polyimide.

Nidan et al. discloses wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As Nidan et al. disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin as taught by Nidan et al. since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

In re claim 16, as applied to claim 7 above, Shimizu et al. in combination with Nidan et al. discloses all claimed limitations including the limitation wherein the first electrically insulating material has a low viscosity (see page 3, paragraph [0070] of Nidan et al.).

In re claim 18, as applied to claim 13 above, Shimizu et al. in combination with Nidan et al. discloses all claimed limitations including the limitation wherein the first electrically insulating material has a low viscosity (see page 3, paragraph [0070] of Nidan et al.).

4. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072), both of record, as applied to claims 7, 16, 13, and 18 above, and further in view of Sakamoto et al. (U.S. Pub. 2004/0014317), newly discovered.

In re claim 17, as applied to claim 16, Paragraph 3 above, Shimizu et al. in combination with Nidan et al. disclose all the claimed limitations including wherein the first electrically insulating material has a predetermined viscosity range (see page 3, paragraph [0070] of Nidan et al.).

However, neither Shimizu et al. nor Nidan et al. specifically disclose that the first electrically insulating material has a viscosity  $\nu$  such that  $\nu \leq 1.0$  Pa·s.

Sakamoto et al. disclose an electrically insulating material **41** fills gap in a junction between IC chip **20** and UV tape **40** wherein the first electrically insulating material **41** is a polyimide resin having a viscosity  $\nu$  ranging from 0.1 to 50 Pa·s (see page 25, paragraph [0453] and FIG. 53(D)).

As Sakamoto et al. disclosed, one of ordinary skill in the art would have been motivated to provide a first electrically insulating material (polyimide resin) having a viscosity  $\nu$  such that  $\nu \leq 1.0$  Pa·s in order to seal the electronic components so as to protect the electronic components (see page 1, paragraph [0007] of Sakamoto et al.). As known to one of ordinary skill in the art, polyimide resin is preferred to be used for sealing and filling

gaps between electronic components because of its viscosity stability, long-term preservability and moisture resistance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. and Nidan et al. references with the polyimide resin of low viscosity  $\nu$  (0.1 to 50 Pa·s) as taught by Sakamoto et al. in order to seal the electronic components so as to protect the electronic components (see page 1, paragraph [0007] of Sakamoto et al.) and furthermore, polyimide resin is preferred to be used for sealing and filling gaps between electronic components because of its viscosity stability, long-term preservability and moisture resistance.

***Allowable Subject Matter***

5. Claims 14-15 were previously indicated as allowable over prior art of record in Office Action mailed on March 19<sup>th</sup>, 2008.
6. Claims 9-12 were previously indicated as objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (see Office Action mailed on March 19<sup>th</sup>, 2008).

***Response to Applicants' Amendment and Arguments***

7. Applicants' arguments filed on January 02<sup>nd</sup>, 2009 have been fully considered but they are not persuasive.

With respect to claims 7 and 13, Applicants contend,

"...in Applicants' claimed embodiment, the polyimide has a low viscosity so that the material can fill any air gaps between the layers. Nidan, in contrast, discloses the use of a polyimide material with a high viscosity as a filler between a sensor chip and a stem so that the material does not flow out from between the chip and the stem."....Applicants further contend that "...One of ordinary skill would not have looked to Nidan to remedy the deficiencies of Shimizu as alleged. For one, "Nidan is not directed to a power semiconductor device, but rather a pressure sensor. As such, there is seemingly no nexus between the two devices or disclosures that would lead one of ordinary skill to combine their respective teachings..."

In response to Applicants' contention that there is no motivation to combine Shimizu et al. and Nidan et al. references, Examiner respectfully disagrees.

It is respectfully submitted that Shimizu et al. disclose all claimed limitations including a first electrically insulating material composed of epoxy resin (see col. 12, lines 49-58) except showing that the electrically insulating material is composed of polyimide.

However, Nidan et al. is being used as a secondary reference to show that materials such as epoxy resin and polyimide resin are interchangeable for sealing and filling purposes in electronic device components.

Regarding about Applicants' contention that there is seemingly no nexus between the two devices or disclosures that would lead one of ordinary

skill to combine their respective teachings because the device of Nidan et al. is not directed to a power semiconductor device.

However, it is respectfully submitted that the combination of Nidan et al. into Shimizu et al. does not change the device operation of Shimizu et al. but rather replacing the sealing material so that it provides better protection for the electronic device components. Nidan et al. provides evidence that epoxy resin and polyimide resin can be substitute for sealing and filling purposes.

With respect to Applicants' contention "...In Applicants' claimed embodiment, the polyimide has a low viscosity so that the material can fill any air gaps between the layers. Nidan, in contrast, discloses the use of a polyimide material with a high viscosity as a filler between a sensor chip and a stem so that the material does not flow out from between the chip and the stem."

However, it is respectfully submitted that Applicants' claimed invention as recited in independent claims 7 and 13 does not clearly specify the viscosity ranges of the polyimide material. The term "low viscosity" alone can not determined fillability of the material into gap or junction between electronic device components. The polyimide resin of Nidan et al. only become high viscosity after being solidified by heat (see page 3, paragraph [0070]). However, during the sealing and filling process, the polyimide resin

having low viscosity thus allowed the polyimide resin material to travel into the gap between the electronic device components.

In view of the above, it is respectfully submitted that it would have been obvious to one having ordinary skill in the art to replace the first electrically insulating material (epoxy resin) of Shimizu et al. with the polyimide resin as taught by Nidan et al. because Nidan et al. provide evidence that these materials can be interchangeable for sealing and filling purposes to better protect electronic device components.

For this reason, Examiner holds the rejection proper.

### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action.

In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Correspondence***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/  
Examiner, Art Unit 2823  
March 06<sup>th</sup>, 2009

/W. David Coleman/  
Primary Examiner, Art Unit 2823